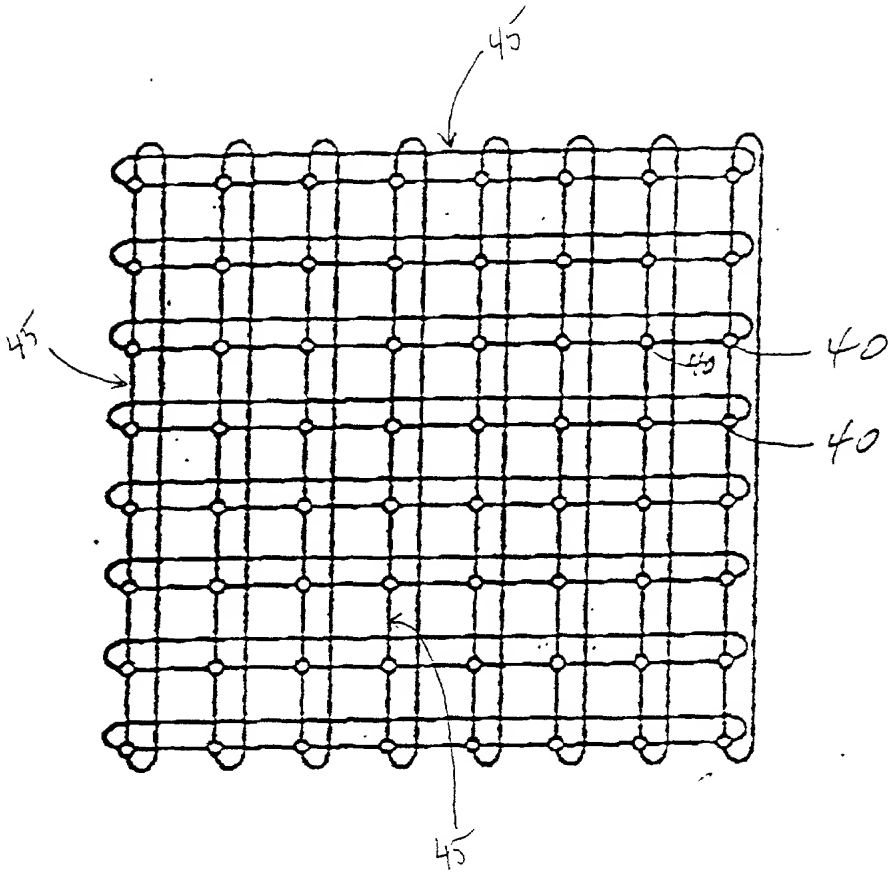


FIG. 1

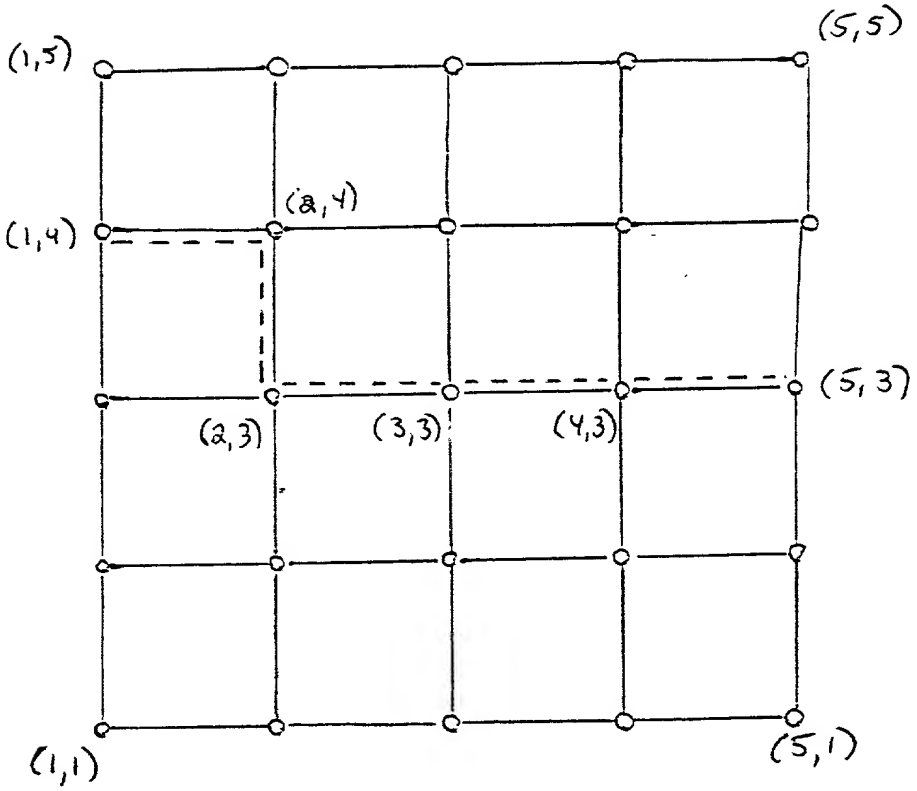


FIG. 2

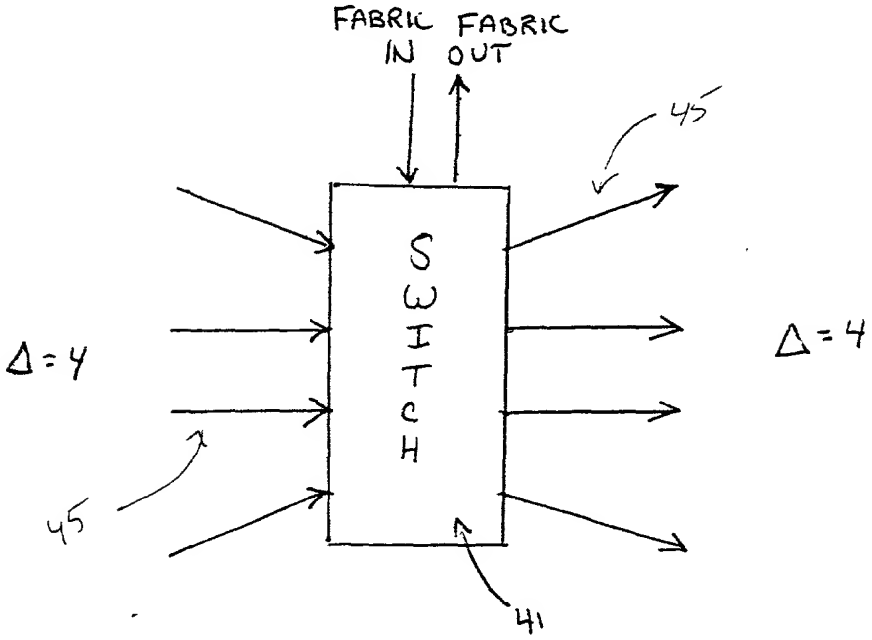


FIG. 3

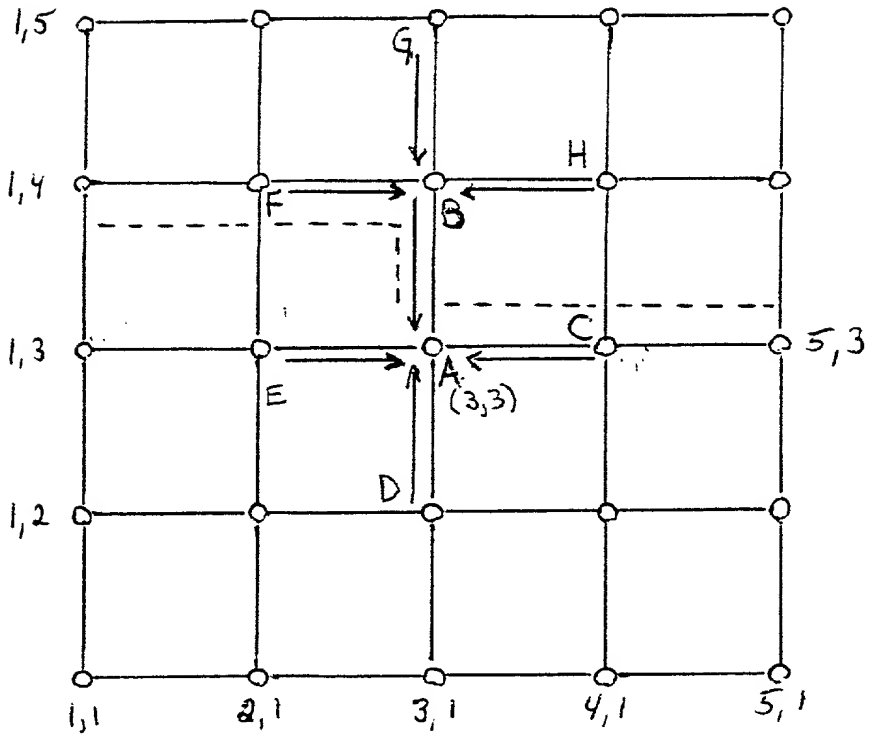
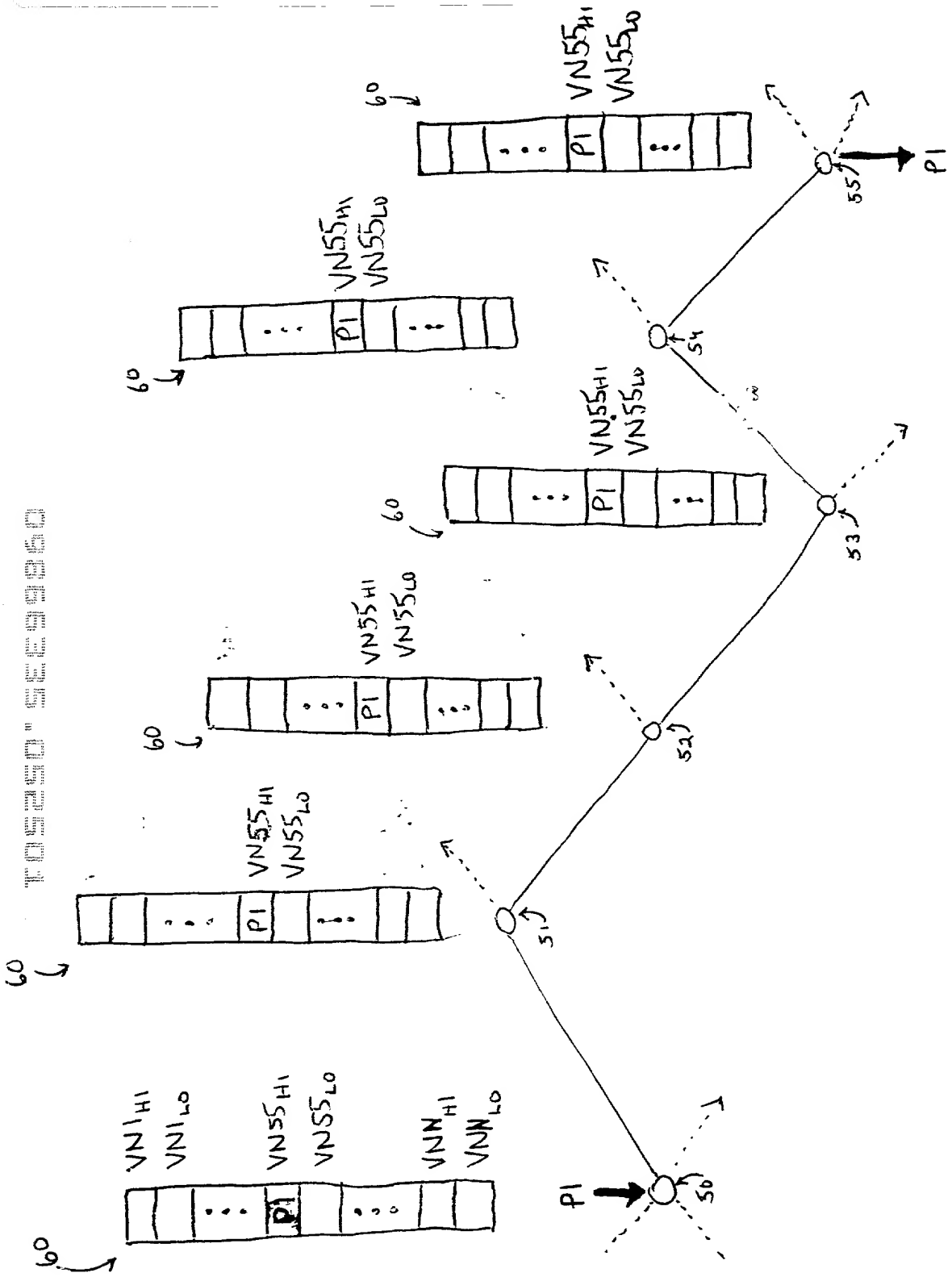


FIG. 4



PRIOR ART

FIG. 5

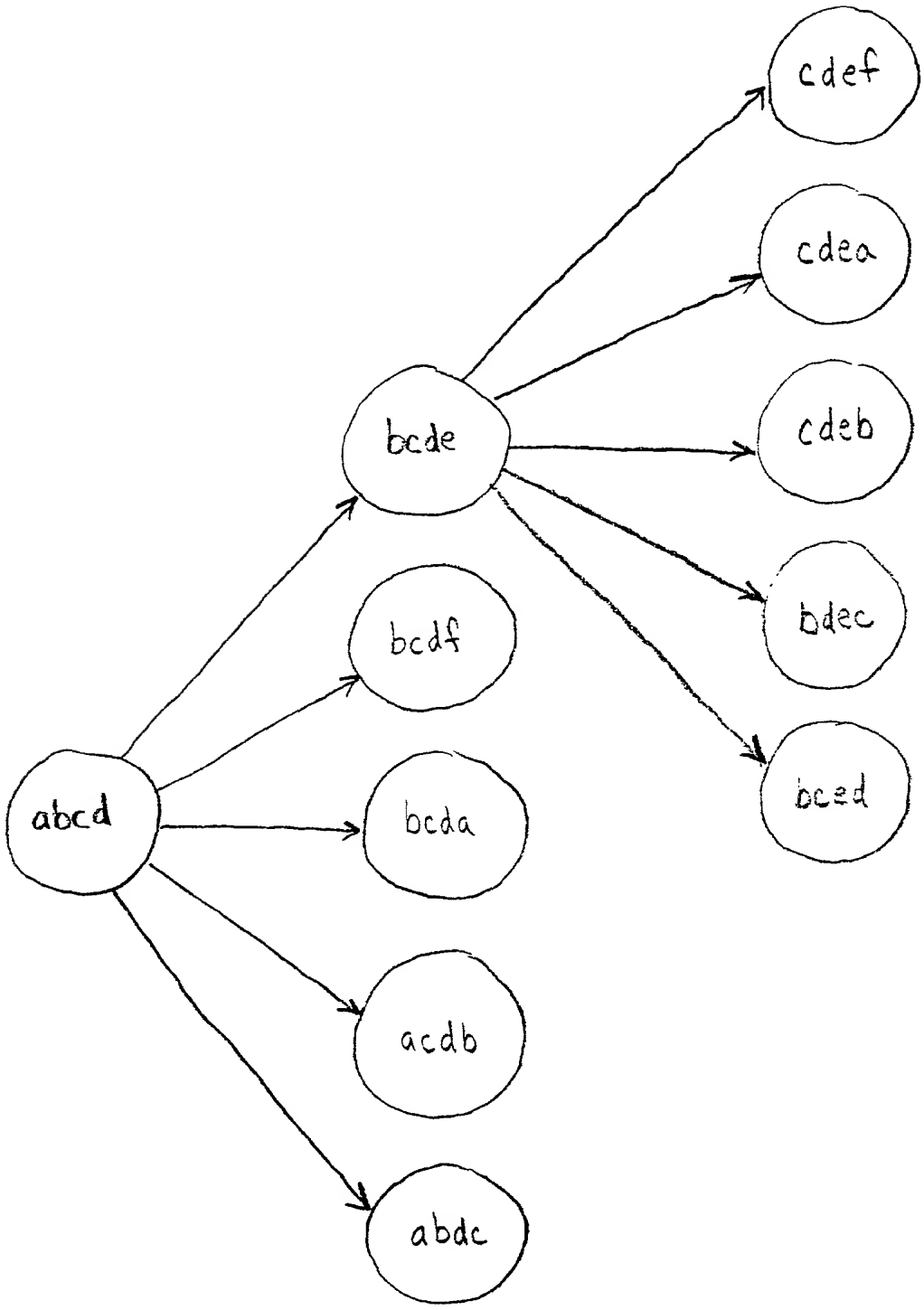


FIG. 6A

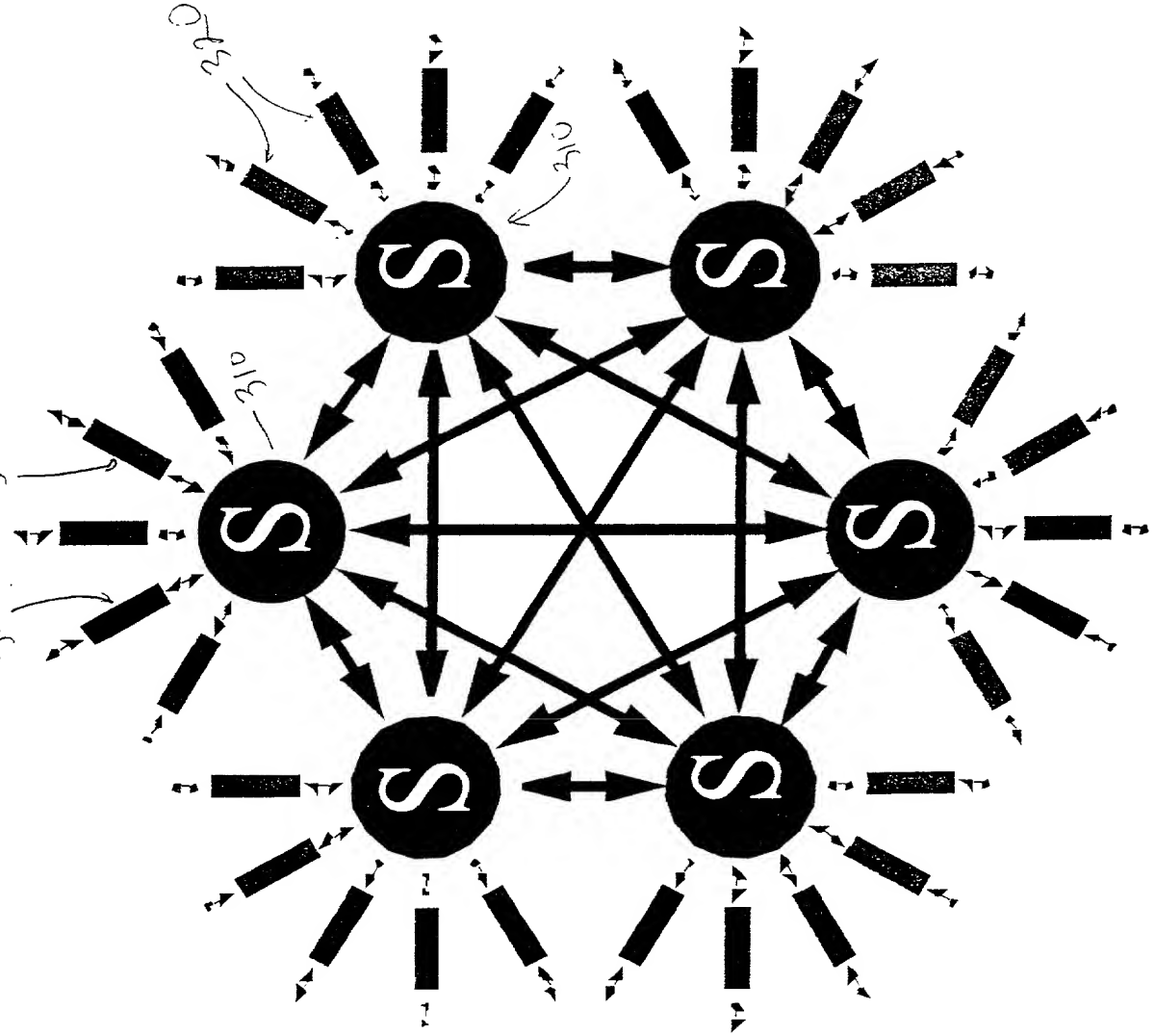


FIG. 6B

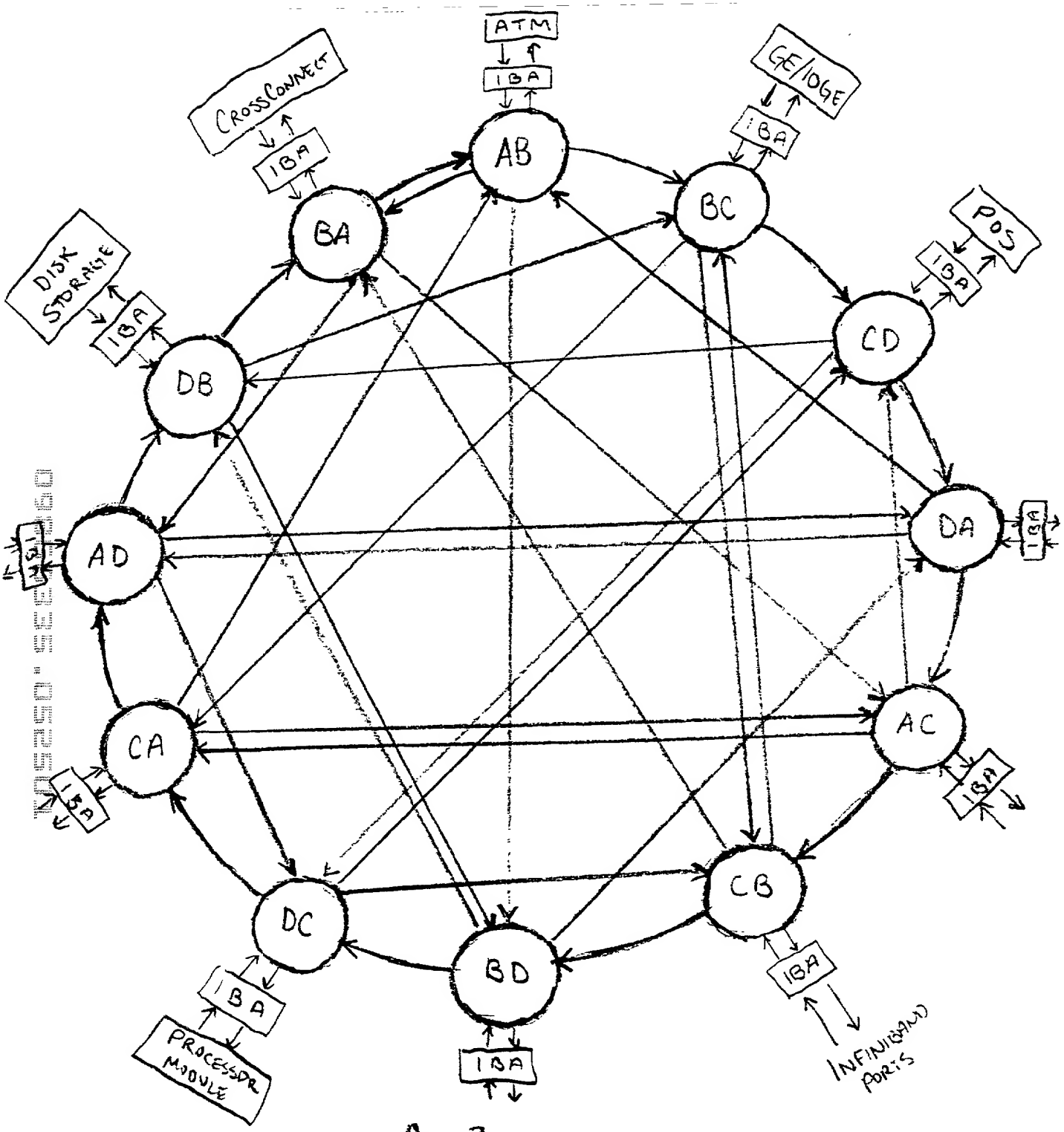

ATM
IBA
CROSSCONNECT
IBA
GE/10GE
IBA
AB
BA
BC
DISK STORAGE
IBA
POS
IBA
DB
CD
AD
DA
IBA
CA
AC
IBA
IBA
CB
DC
BD
IBA
IBA
PROCESSOR MODULE
IBA
INFINIBAND PORTS
Δ = 3
D = 2

FIG. 7A

ADJACENCY TABLES FOR NODES IN FIG. 7A

AB	**AC**	**AD**
AB → BC	AC → CB	AD → DB
AB → BD	AC → CD	AD → DC
AB → BA	AC → CA	AD → DA
BA	**BC**	**BD**
BA → AC	BC → CD	BD → DA
BA → AD	BC → CA	BD → DC
BA → AB	BC → CB	BD → DB
CA	**CB**	**CD**
CA → AB	CB → BD	CD → DA
CA → AD	CB → BA	CD → DB
CA → AC	CB → BC	CD → DC
DA	**DB**	**DC**
DA →AB	DB → BA	DC → CA
DA →AC	DB → BC	DC → CB
DA →AD	DB → BD	DC → CD

FIG. 7B

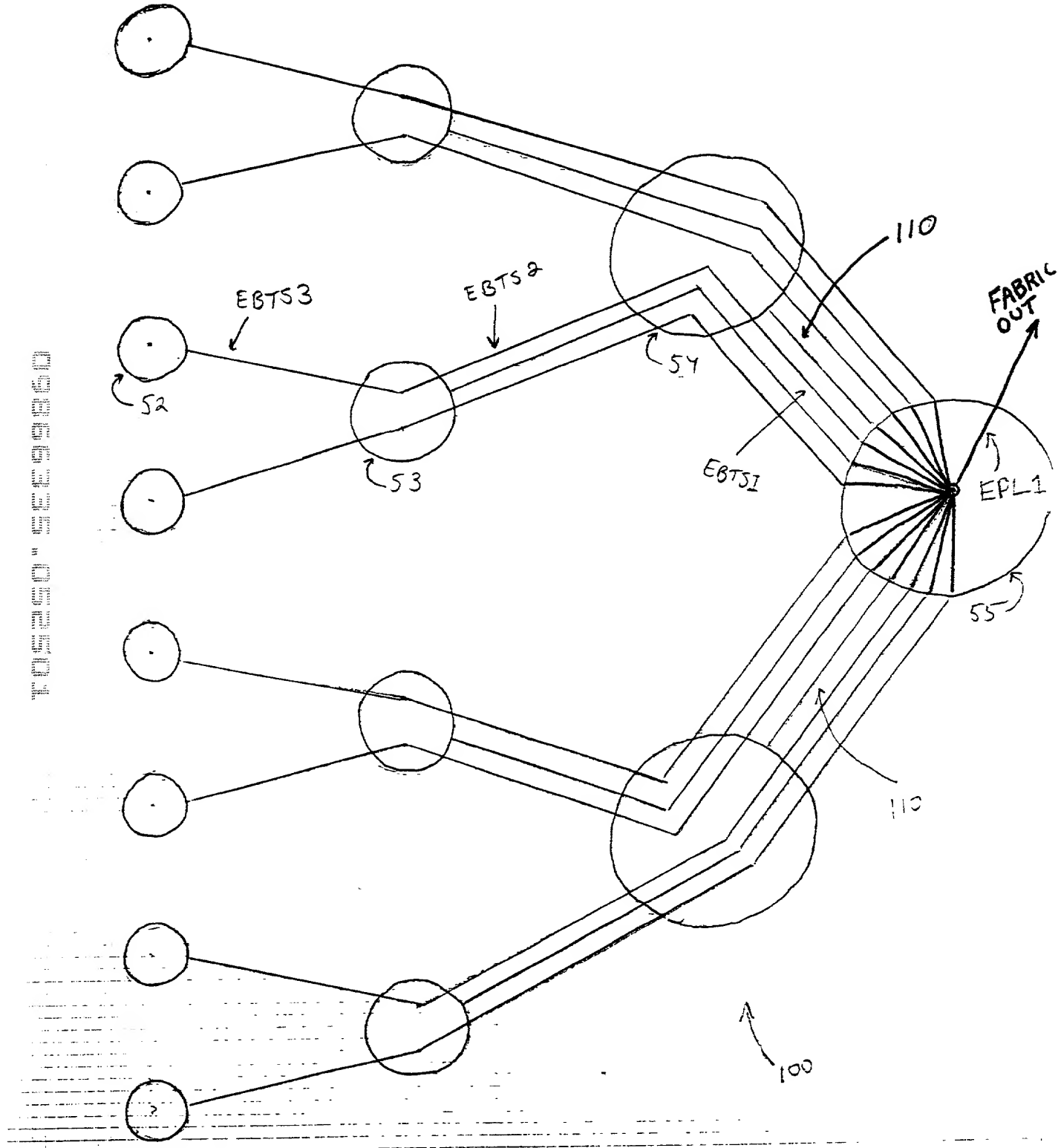


FIG. 8A

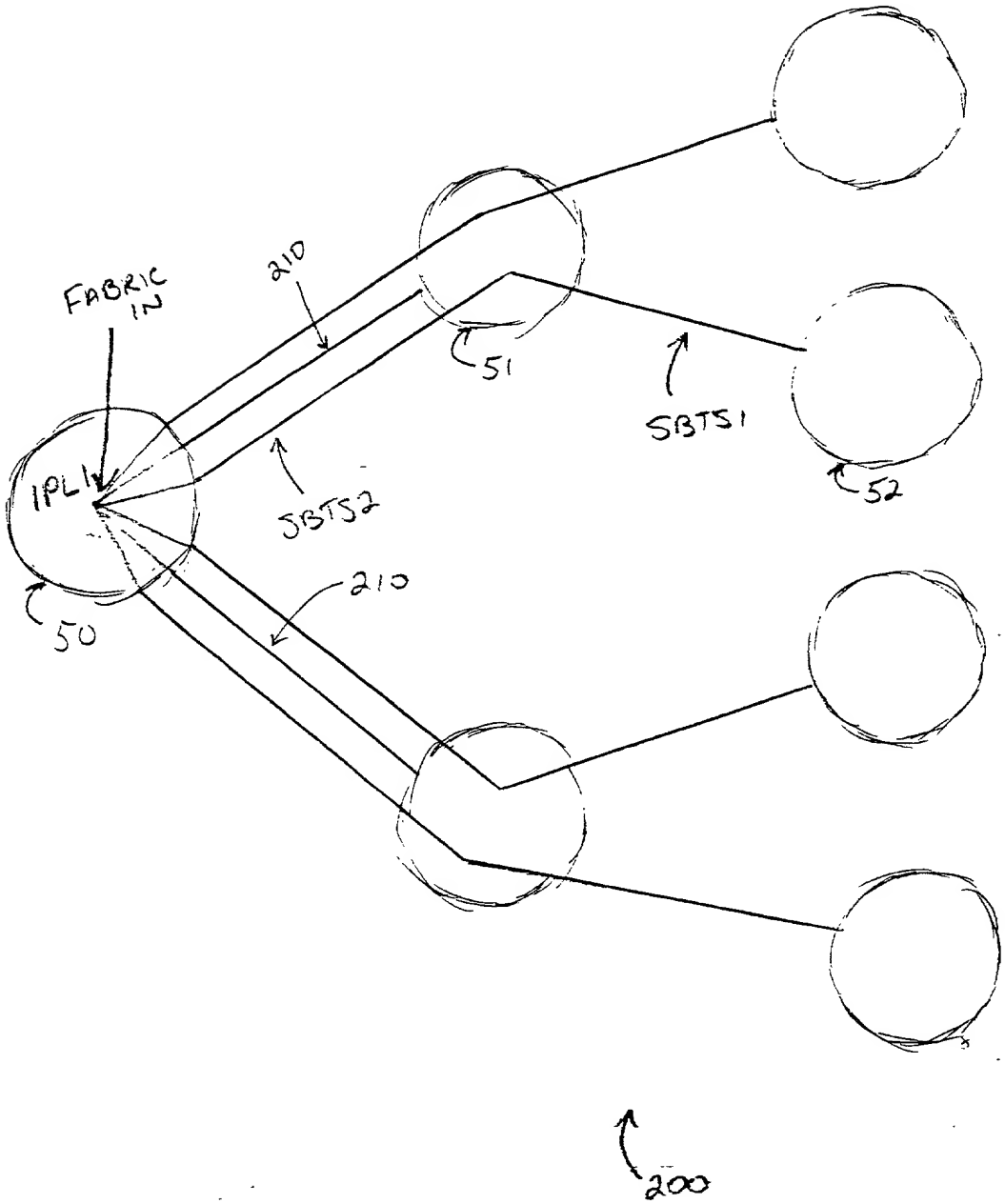


FIG. 8B

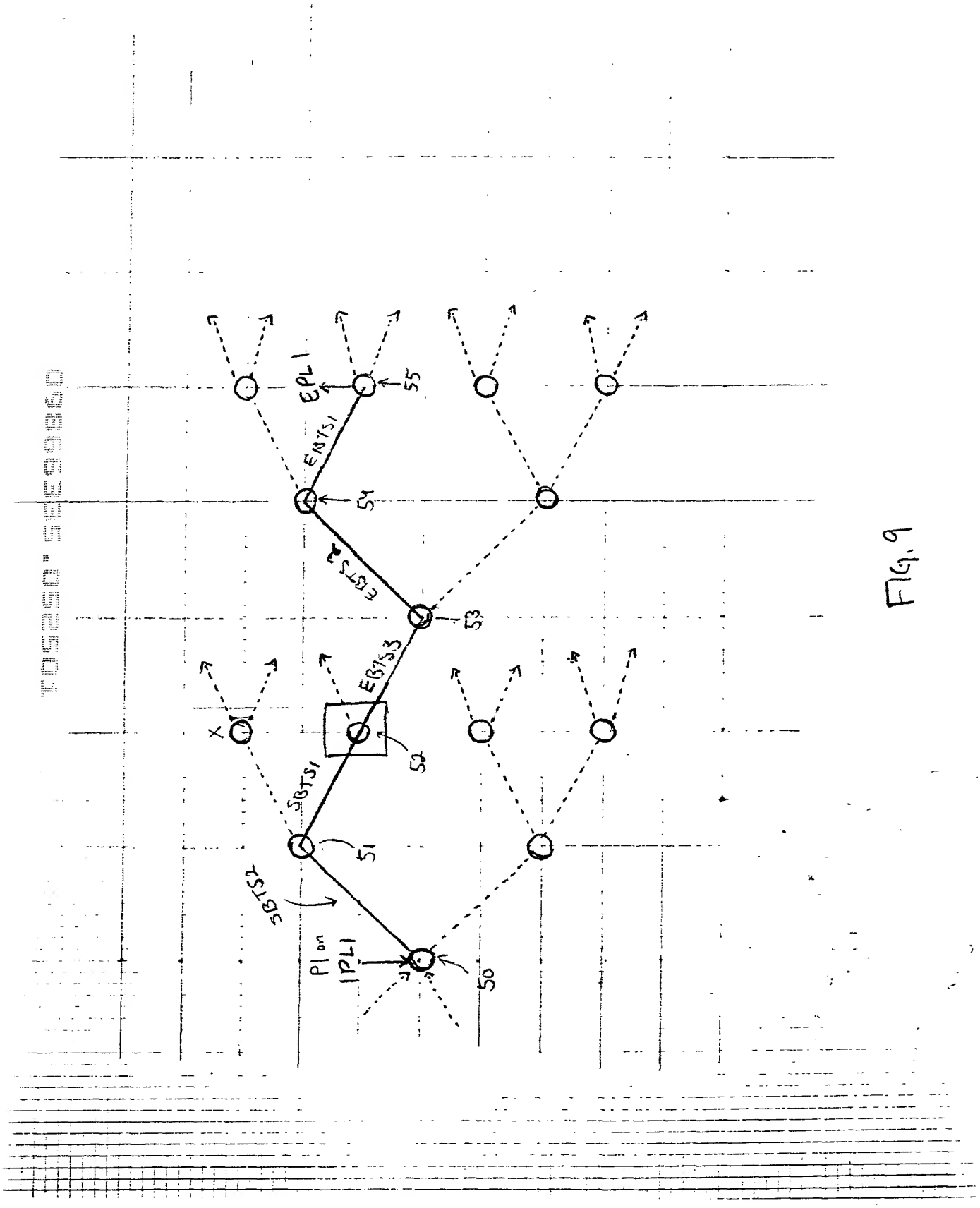


Fig. 9

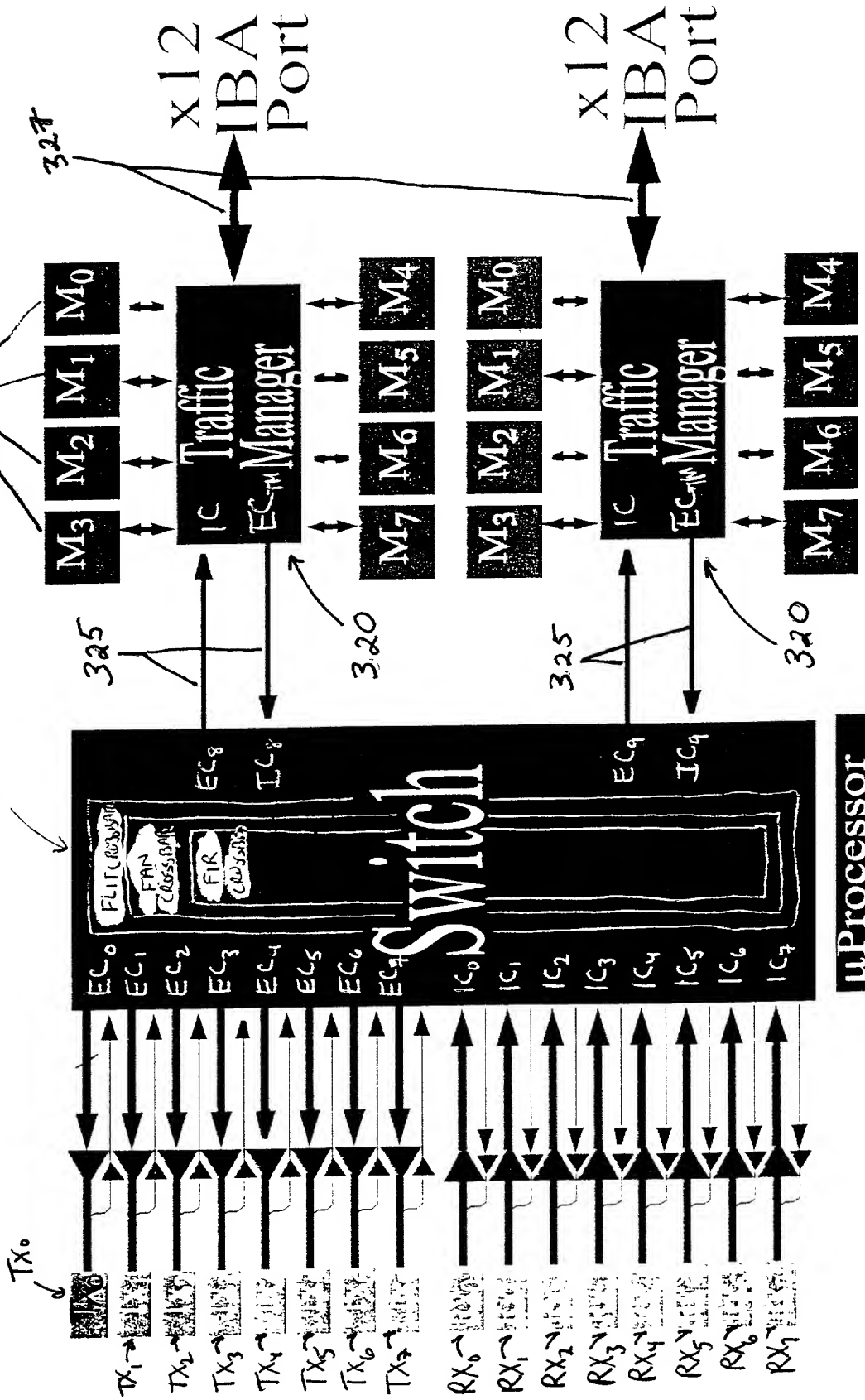

x12 IBA Port
x12 IBA Port
Traffic Manager
Traffic Manager
Switch
µProcessor Manager
FLIT
FAP Crossbar
FIR
M0
M1
M2
M3
M4
M5
M6
M7
EC0
EC1
EC2
EC3
EC4
EC5
EC6
EC7
EC8
EC9
IC0
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
TX0
TX1
TX2
TX3
TX4
TX5
TX6
TX7
RX0
RX1
RX2
RX3
RX4
RX5
RX6
RX7
310
320
325
327
330
340

FIG. 10

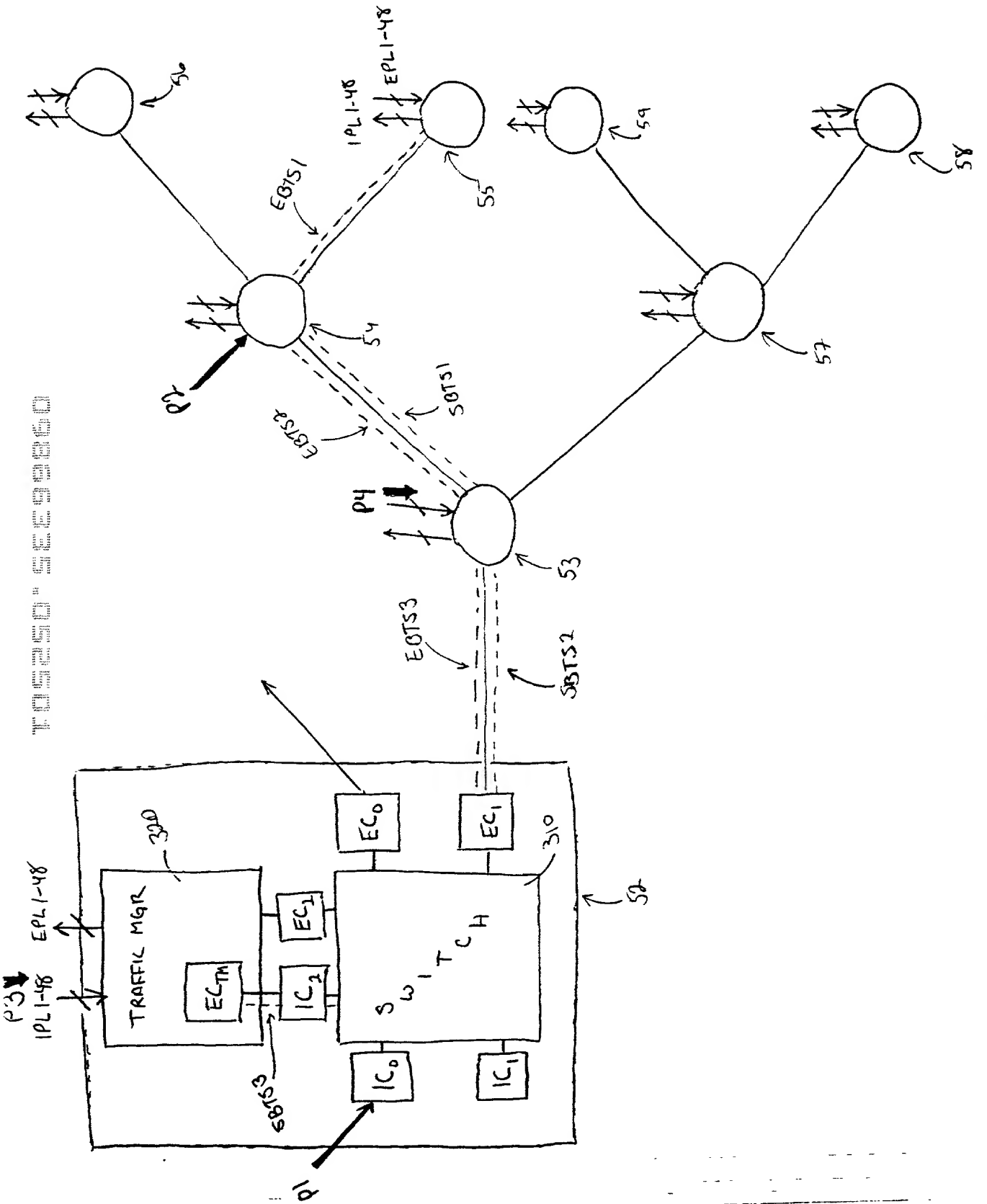

56
IPL1-48
EPL1-48
EGTS1
55
59
58
54
57
P2
EGTS2
SGTS1
P4
53
EGTS3
SGTS2
EC0
EC1
310
320
TRAFFIC MGR
EPL1-48
P3
IPL1-48
EC1
ECTM
IC2
SWITCH
52
SGTS3
IC0
IC1
P1

FIG. 11A

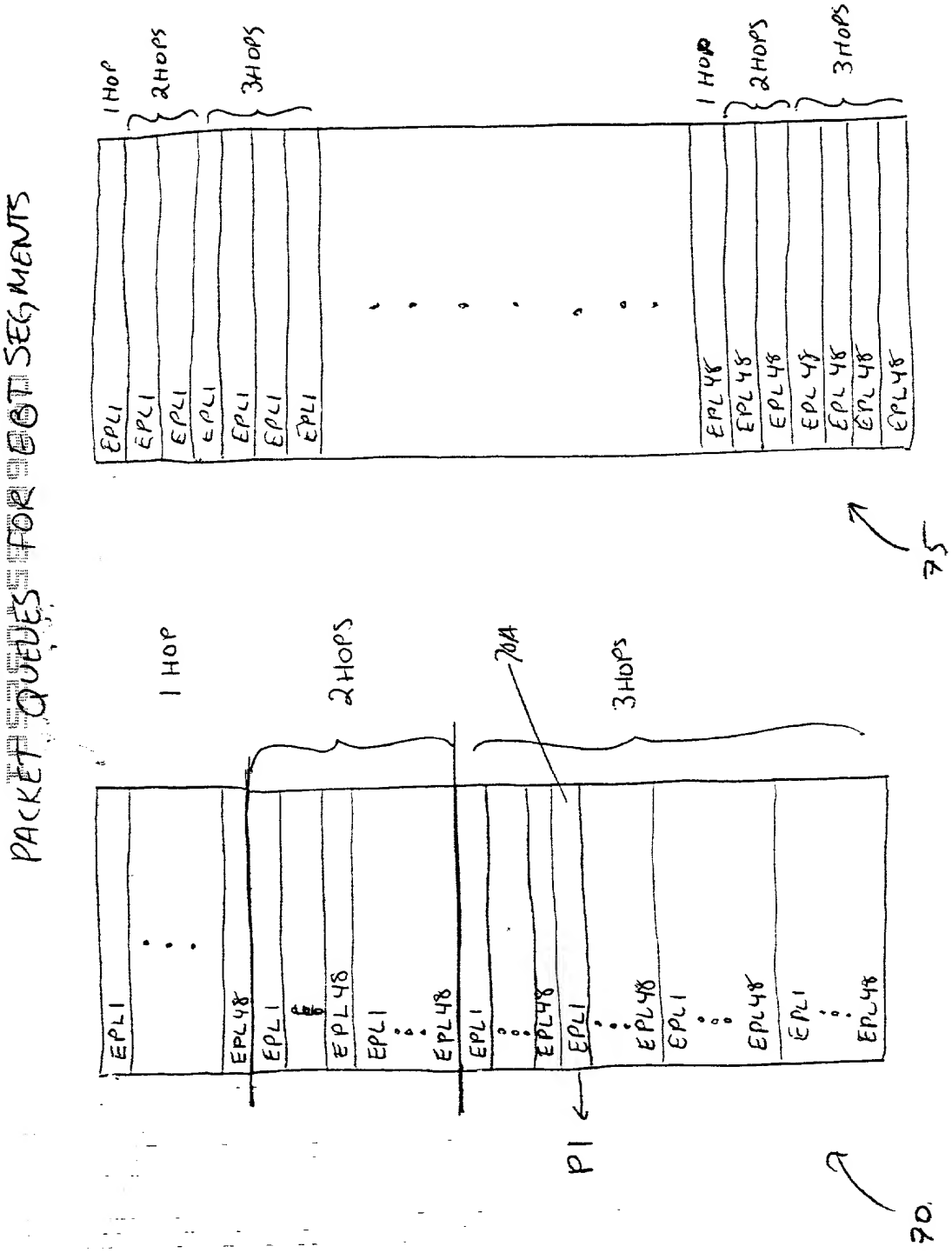


FIG. 11A

FIG. 11C

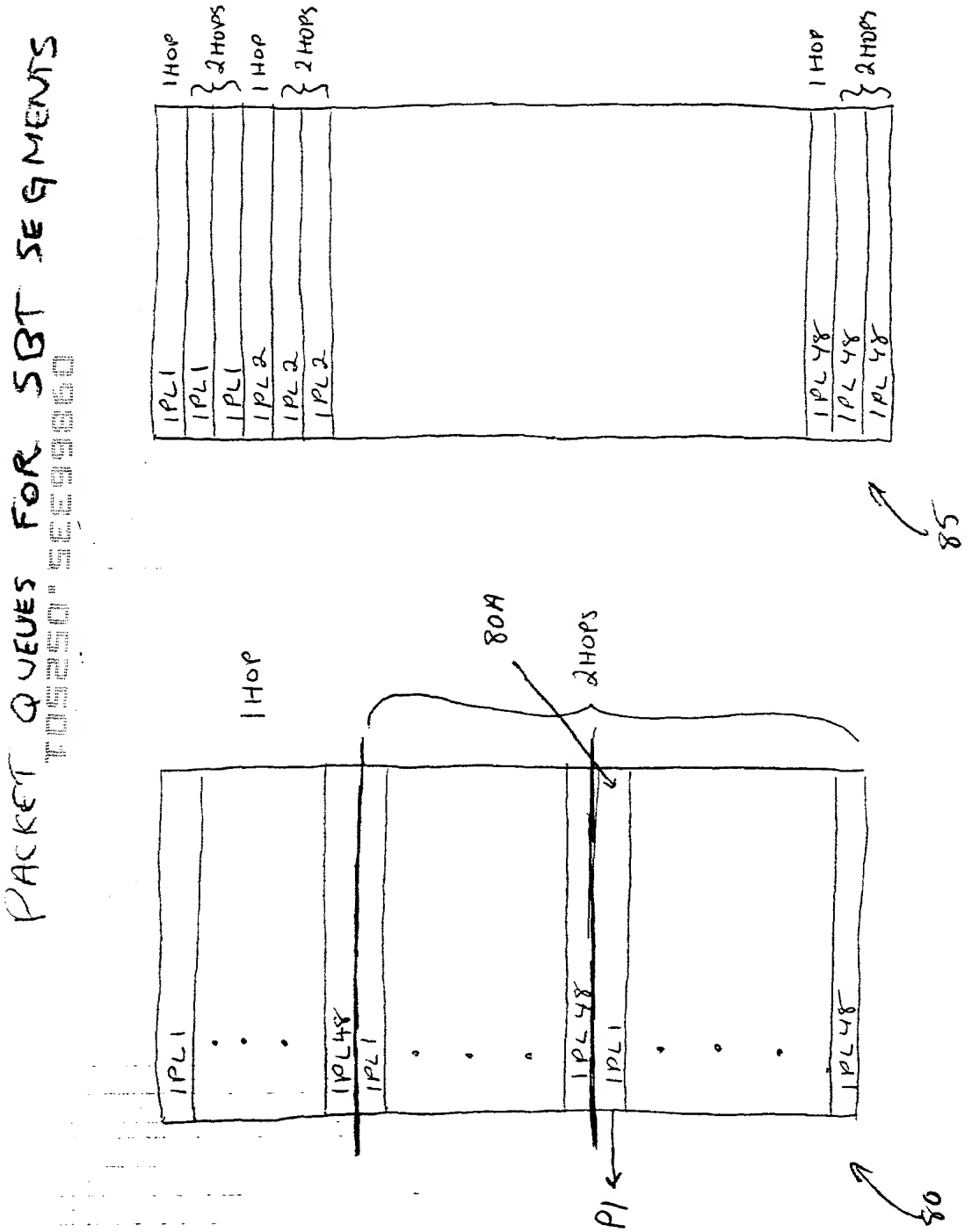


FIG. 11E

FIG. 11D

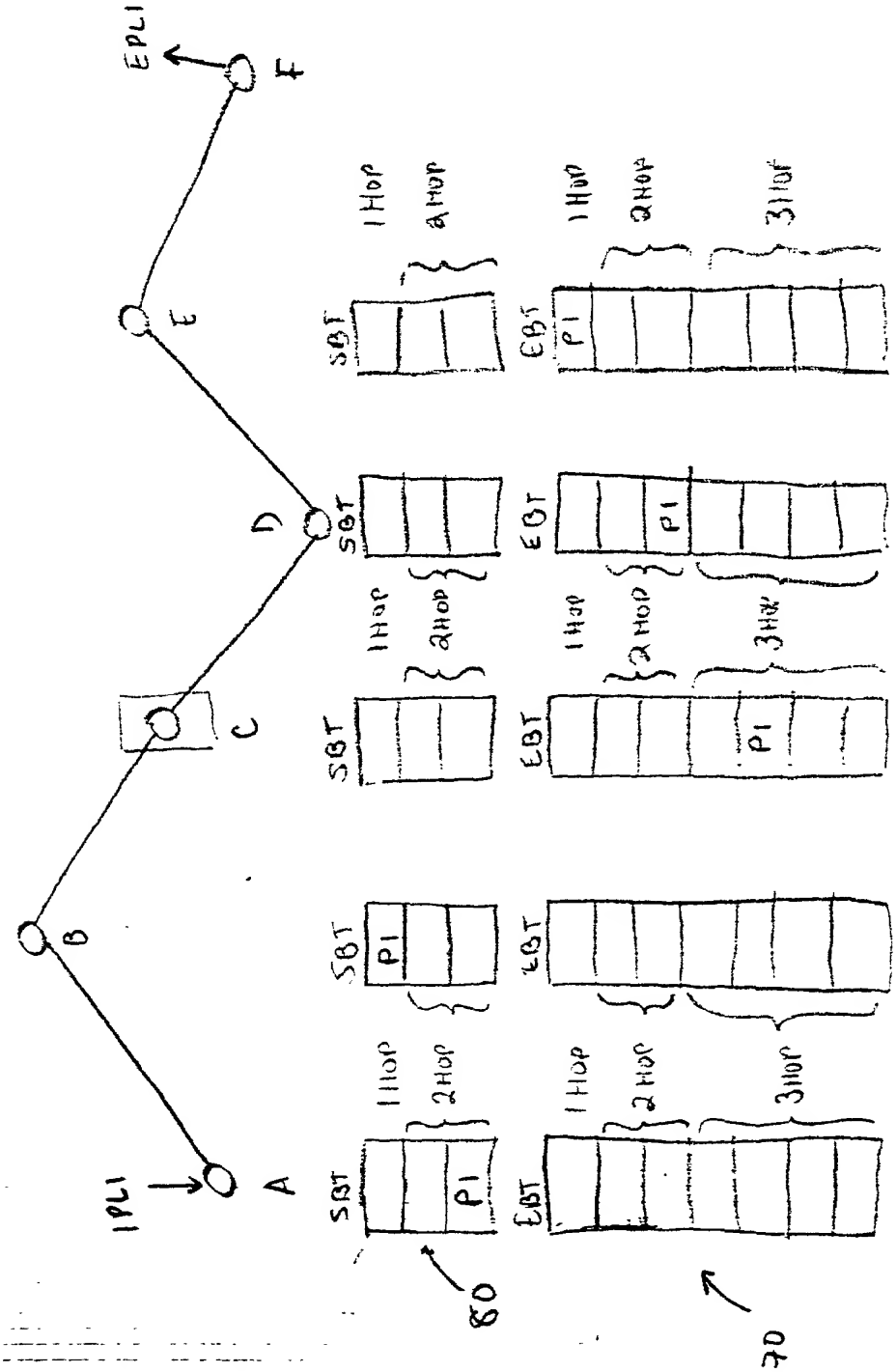


Fig 11F

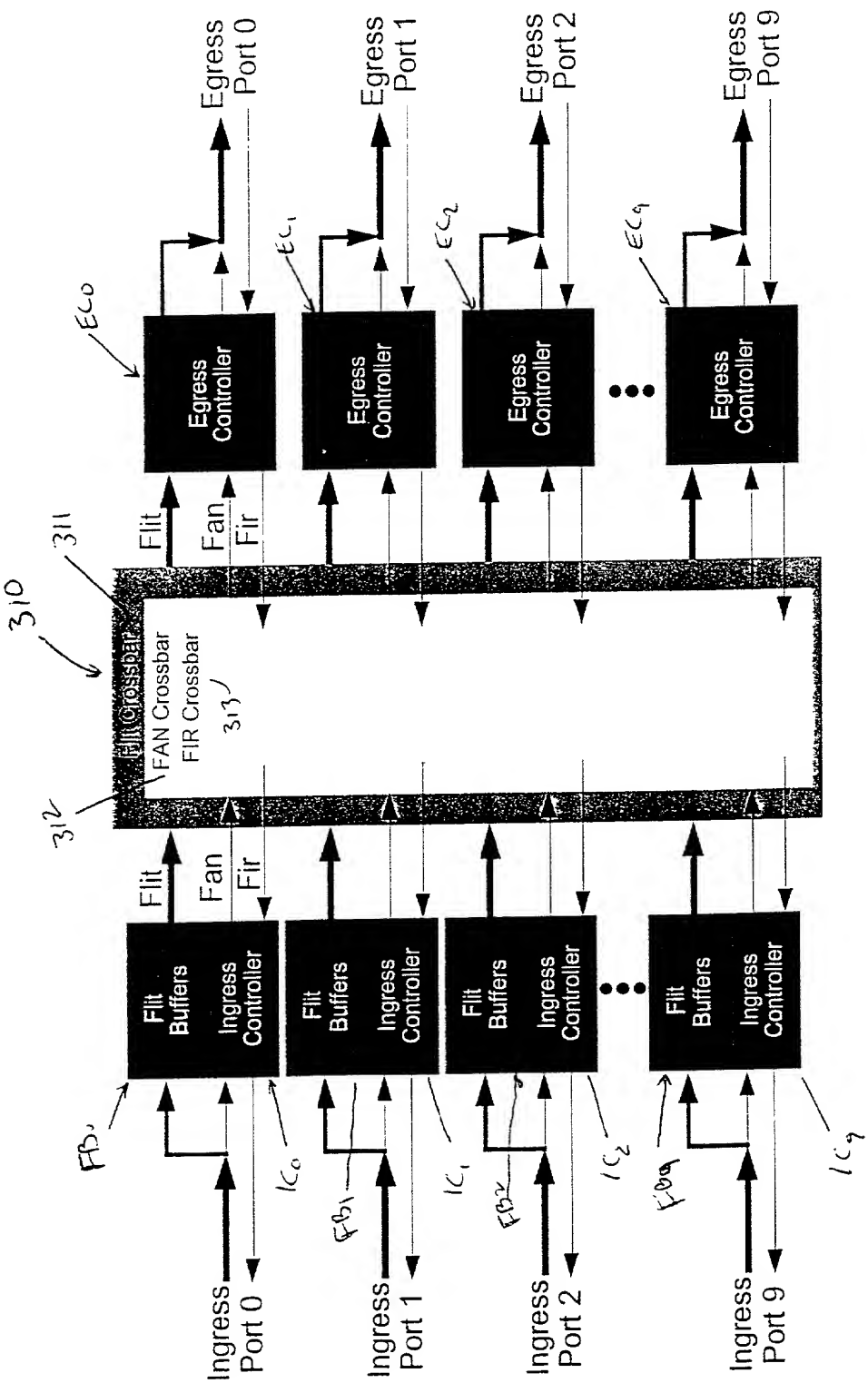

Egress Port 0
Egress Port 1
Egress Port 2
Egress Port 9
Egress Controller
EC0
EC1
EC2
EC9
310
311
312
313
FIR Crossbar
FAN Crossbar
FIR Crossbar
Flit
Fan
Fir
Flit Buffers
Ingress Controller
FB0
FB1
FB2
FB9
IC0
IC1
IC2
IC9
Ingress Port 0
Ingress Port 1
Ingress Port 2
Ingress Port 9

Fig. 12

CONTROL STRUCTURE	SIZE (IN BITS)	DESCRIPTION
IngressPacketState	1280x35=44,800	Each IngressPacketState structure manages the storage of a partially received packet on one of the ingress ports.
EgressLaneState	(128x30=3,480)	Each EgresslaneState structure supplies information used to process received Credits.
AvailableEgressLane	(128x1)	Each flag indicates that a particular lane is available or in use.
FanState	(512x44=22,528)	Each FanState structure holds one FAN waiting to be converted into a FIR and pointers which allow creating a linked list of packets waiting on a particular channel and a linked list of FANs comprising a particular packet.
AvailableFanState	(512x1)	Each flag indicates that a particular local FanState structure is availably or in use.
WaitingForlanes	(2928x1)	Each flag indicates that a particular tunnel segment has a packet ready to be assigned to a lane as soon as one becomes available.
WaitingForFSM	(2928x1)	Each flag indicates that a particular channel has a FAN ready to be converted into a FIR as soon as the EgressController has bandwidth available to perform the conversion.
WaitingForFirFifo	(2304x1)	Each flag indicates that a particular lane has a FAN ready to convert into a FIR as soon as room in the FIR FIFO becomes non-full.
SegmentPointer	(2938x13=38,194)	Each SegmentPointer points to a a queue of packets waiting on a tunnel segment.

FIG. 13

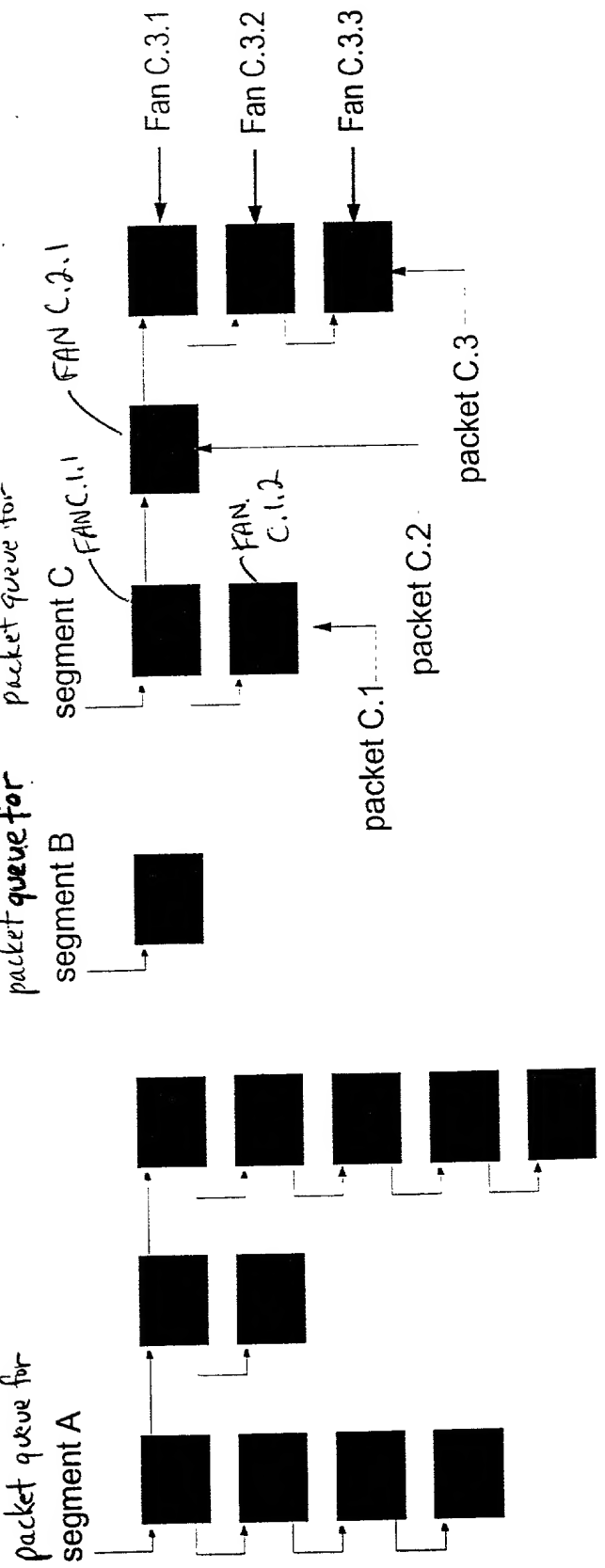

Fan C.3.1
Fan C.3.2
Fan C.3.3
FAN C.2.1
packet C.3
packet queue for
segment C
FAN C.1.1
FAN C.1.2
packet C.2
packet C.1
packet queue for
segment B
packet queue for
segment A

FIG. 14

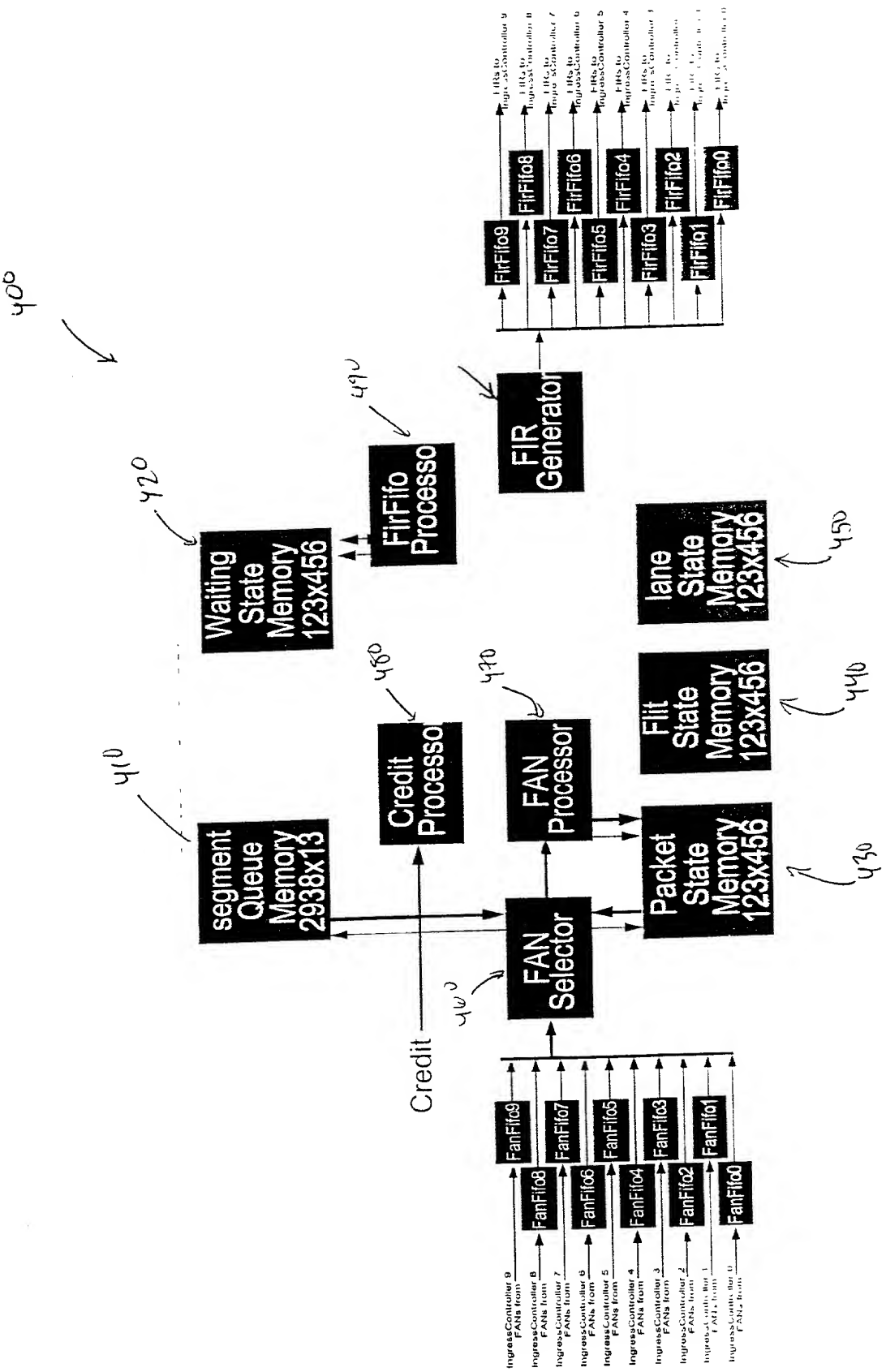

400
410
420
430
440
450
460
470
480
490
segment Queue Memory 2938x13
Waiting State Memory 123x456
Packet State Memory 123x456
Flit State Memory 123x456
Iane State Memory 123x456
Credit Processo
FAN Processor
FirFifo Processo
FIR Generator
FAN Selector
Credit
FirFifo9
FirFifo8
FirFifo7
FirFifo6
FirFifo5
FirFifo4
FirFifo3
FirFifo2
FirFifo1
FirFifo0
FanFifo9
FanFifo8
FanFifo7
FanFifo6
FanFifo5
FanFifo4
FanFifo3
FanFifo2
FanFifo1
FanFifo0

Fig. 15